LISTING OF THE CLAIMS

This listing of claims replaces all prior versions.

1. (Currently Amended) A semiconductor device having opposed first and second major surfaces, comprising:

a body region in a substrate at the first major surface;

a plurality of ~~at least one~~ cells each having longitudinally spaced source and drain implantations extending into the body region from the first major surface, each of the source and drain implantations being spaced away from the substrate by part of the body region and defining a channel part of the body region between the respective source and drain implantations, the source implantations of the cells not being formed by a common region and the drain implantations of the cells not being formed by a common region; and

for each of the cells, an ~~at least one~~ insulated gate trench extending longitudinally from the source implantation of the cell to the drain implantation of the cell through the body region, the insulated gate trench including a gate conductor insulated from the source and drain implantations of the cell and the body region by a gate dielectric along the side and end walls and the base of the gate trench, the source and drain implantations of the cell extending along part of the side walls of the gate trench,

wherein the source and drain implantations of each cell include conductive shallow contact regions at the first major surface extending vertically into the body to a depth of no more than 35% of the depth of the trench.

2. (Original) A semiconductor device according to claim 1 wherein the body region is of first conductivity type and the shallow contact regions are of a second conductivity type opposite to the first conductivity type.

3. (Previously presented) A semiconductor device according to claim 1 or 2 wherein each of the source and drain implantations further comprises a lower doped region of lower doping than the shallow contact region.

4. (Currently Amended) A semiconductor device according to claim 3, wherein, for each of the cells:

the source implantation includes a higher doped shallow source contact region and a lower doped source drift region between the higher doped source contact region and the body;

the drain implantation includes a higher doped shallow drain contact region and a lower doped drain drift region between the higher doped drain contact region and the body;

the insulated gate trench includes potential plate regions extending longitudinally on either side of a central region, the potential plate regions being adjacent to the source and drain drift regions respectively, and the central region being adjacent to the body; and

the thickness of the gate dielectric sidewalls of the insulated gate trench is greater in the potential plate regions of the insulated gate than the central region.

5. (Currently Amended) A semiconductor device according to claim 1, further comprising:

a gate electrode that is electrically connected to each of the gate trenches;

a source electrode that is electrically connected to the conductive shallow regions of the source implantations of each of the cells; and

a drain electrode that is electrically connected to the conductive shallow regions of the drain implantations of each of the cells ~~a plurality of cells laterally spaced across the first major surface~~.

6. (Currently Amended) A semiconductor device according to claim 1 [[5]] wherein gate trenches alternate with the plurality of cells laterally across the first major surface.

7. (Currently Amended) A semiconductor device according to claim 1 [[5]] wherein each of the cells has one of the [[a]] gate trenches laterally within the confines of the cell.

8. (Previously presented) A semiconductor device according to claim 3 wherein the lower doped region of lower doping than the shallow contact region extends vertically below the shallow contact region to a depth at least 80% of the depth of the trench.

9. (Previously presented) A semiconductor device according to claim 1, wherein the source and drain implantations consist exclusively of the shallow contact region.

10. (Previously presented) A semiconductor device according to claim 1 on a conductive substrate of first conductivity type.

11. (Previously Presented) A semiconductor device having opposed first and second major surfaces, comprising:

a body region in a substrate at the first major surface;

at least one cell having longitudinally spaced source and drain implantations extending into the body region from the first major surface, the source and drain implantations being spaced away from the substrate by part of the body region and defining a channel part of the body region between the source and drain implantations; and

at least one insulated gate trench extending longitudinally from the source implantation to the drain implantation through the body region, the insulated gate trench including a gate conductor insulated from the source and drain implantations and the body region by a gate dielectric along the side and end walls and the base of the trench, the source and drain implantations extending along part of the side walls of the trench,

wherein the source and drain implantations include conductive shallow contact regions at the first major surface extending vertically into the body to a depth of no more than 35% of the depth of the trench, and

wherein the gate dielectric along the side and end walls of the trench is in contact with the gate conductor, the source and drain implantations and the respective shallow contact regions of the source and drain implantations.

12. (Previously Presented) A semiconductor device having opposed first and second major surfaces, comprising:

a body region in a substrate at the first major surface;

at least one cell having longitudinally spaced source and drain implantations extending into the body region from the first major surface, the source and drain implantations being spaced away from the substrate by part of the body region and defining a channel part of the body region between the source and drain implantations; and

at least one insulated gate trench extending longitudinally from the source implantation to the drain implantation through the body region, the insulated gate trench including a gate conductor insulated from the source and drain implantations and the body region by a gate dielectric along the side and end walls and the base of the trench, the source and drain implantations extending along part of the side walls of the trench,

wherein the source and drain implantations include conductive shallow contact regions at the first major surface extending vertically into the body to a depth of no more than 35% of the depth of the trench, and

wherein the insulated gate trench includes end portions extending into the source and drain implantations, with each of the source and drain implantations having portions thereof laterally adjacent to an endwall and opposing sidewalls of the trench to surround the end portion of the trench on three sides.

13. (Previously presented) A semiconductor device comprising:

a body having an upper surface;

a source region in the body below the upper surface;

a drain region in the body below the upper surface;

a gate trench region extending laterally in the body below the upper surface, and having opposing ends respectively into the source region and the drain region, the gate trench region including

a gate dielectric material on sidewalls, endwalls and a bottom of the trench, the dielectric material at each end of the gate trench region being in contact with

each of the respective source and drain regions on respective opposing endwalls and sidewalls of the trench,

a gate electrode in the trench and in contact with the gate dielectric material, and being separated from the respective source and drain regions by the dielectric material.

14. (Previously presented) The device of claim 13, wherein

the source region and the drain region respectively include a contact region adjacent to the upper surface, and

the gate trench region extends laterally into the contact region.

15. (New) The device of claim 1, wherein the source and drain implantations of each of the cells are in contact with the gate dielectric along the end walls of one of the gate trenches.

16. (New) The device of claim 1, wherein each of the gate trenches extends into the source and drain implantations of one of the cells.